In the Claims

Applicant has submitted a new complete claim set showing marked up claims with insertions indicated by underlining and deletions indicated by strikeouts and/or double bracketing.

Please amend pending claims 1, 21, 22 and 42 as noted below.

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1. (Currently amended) A microcomputer comprising:

at least one processor;

a debug circuit;

a system bus coupling the processor and debug circuit; and

a communication link coupling the processor and debug circuit, wherein the processor is configured to transmit to the debug circuit through the communication link a plurality of bit values each representing a state of an operation in the processor including at least ~~one of:~~ an operand address.

~~an operand address; and~~

~~an instruction address.~~

2. (Original) The microcomputer according to claim 1, wherein at least one of the plurality of bit values represents a state of an operation in the processor including an operand value and operand address.

3. (Original) The microcomputer according to claim 1, wherein the processor is further configured transmit to the debug circuit a program counter value indicating the program counter of the processor.

4. (Original) The microcomputer according to claim 3, wherein the program counter has a value corresponding to a value of the program counter at a writeback stage of a pipeline of the processor.

5. (Original) The microcomputer according to claim 4, wherein the processor is further configured transmit to the debug circuit a status indicating that a computer instruction is in the writeback stage is a valid computer instruction.

6. (Original) The microcomputer according to claim 4, wherein the processor is further configured transmit to the debug circuit a status indicating that the computer instruction in the writeback stage is a first instruction past a branch instruction.

7. (Original) The microcomputer according to claim 6, wherein the processor is further configured transmit to the debug circuit a status indicating a type of an executed branch instruction.

8. (Original) The microcomputer according to claim 7, wherein the debug circuit is configured to transmit a trace packet indicating the type of the executed branch instruction.

9. (Original) The microcomputer according to claim 1, wherein the plurality of bit values representing a pre-execution state of the processor.

10. (Original) The microcomputer according to claim 1, wherein the processor is configured to suppress transmitting the plurality of bit values upon detecting an exception.

11. (Original) The microcomputer according to claim 1, wherein the processor is further configured transmit to the debug circuit address information of an executed instruction.

12. (Original) The microcomputer according to claim 1, wherein the processor is further configured transmit to the debug circuit data information of an executed instruction.

13. (Original) The microcomputer according to claim 1, wherein the processor is further configured transmit to the debug circuit process identifier information of an executed instruction.

14. (Original) The microcomputer according to claim 1, wherein the debug circuit is capable of transmitting processor control signals, including at least one of:

a signal to suspend operation of the processor;

a signal to resume fetching instructions;

a signal to reset the processor;

a signal to indicate that an exception has occurred in the debug unit.

15. (Original) The microcomputer according to claim 1, wherein at least one of the plurality of bit values represents a match state between a match value and a portion of an executed instruction.

16. (Original) The microcomputer according to claim 1, wherein at least one of the plurality of bit values represents a match state between a match value and a memory address accessed by the processor in response to an executed instruction.

17. (Original) The microcomputer according to claim 1, wherein the processor is further configured transmit to the debug circuit a value indicating an increment of the program counter of the processor.

18. (Original) The microcomputer according to claim 1, wherein the processor is further configured transmit to the debug circuit a value indicating a change in process identifier value.

19. (Original) The microcomputer according to claim 3, wherein the debug circuit is adapted to generate trace information including the program counter.

20. (Original) The microcomputer according to claim 1, wherein the microcomputer is implemented on a single integrated circuit.

21. (Currently amended) A microcomputer implemented on a single integrated circuit, the microcomputer comprising:

at least one processor;

a debug circuit;

a system bus coupling the processor and debug circuit; and

a communication link coupling the processor and debug circuit, wherein the processor is configured to transmit to the debug circuit through the communication link a plurality of bit values each representing a state of an operation in the processor including at least one of:

an operand address; and

~~an instruction address; and~~

an operand value;

wherein the processor is further configured transmit to the debug circuit:

a program counter value indicating the program counter of the processor at a writeback stage of a pipeline of the processor;

a status indicating that a computer instruction is in the writeback stage is a valid computer instruction;

a status indicating that the computer instruction in the writeback stage is a first instruction past an executed branch instruction;

a status indicating a type of the executed branch instruction; and

process identifier information of an executed instruction.

22. (Currently amended) A microcomputer comprising:

at least one processor;

a debug circuit;

a system bus coupling the processor and debug circuit; and

means for transmitting to the debug circuit a plurality of bit values each representing a state of an operation in the processor including at least ~~one of:~~ an operand address.

~~an operand address; and~~

~~an instruction address.~~

23. (Original) The microcomputer according to claim 22, wherein at least one of the plurality of bit values represents a state of an operation in the processor including an operand value and operand address.

24. (Original) The microcomputer according to claim 22, wherein the microcomputer further comprises means for transmitting to the debug circuit a program counter value indicating the program counter of the processor.

25. (Original) The microcomputer according to claim 24, wherein the program counter has a value corresponding to a value of the program counter at a writeback stage of a pipeline of the processor.

26. (Original) The microcomputer according to claim 25, wherein the processor comprises means for transmitting to the debug circuit a status indicating that a computer instruction is in the writeback stage is a valid computer instruction.

27. (Original) The microcomputer according to claim 25, wherein the processor comprises means for transmitting to the debug circuit a status indicating that the computer instruction in the writeback stage is a first instruction past a branch instruction.

28. (Original) The microcomputer according to claim 27, wherein the processor comprises means for transmitting to the debug circuit a status indicating a type of an executed branch instruction.

29. (Original) The microcomputer according to claim 28, wherein the debug circuit includes means for transmitting a trace packet indicating the type of the executed branch instruction.

30. (Original) The microcomputer according to claim 22, wherein the plurality of bit values representing a pre-execution state of the processor.

31. (Original) The microcomputer according to claim 22, wherein the processor includes means for suppressing a transmission of the plurality of bit values upon detecting an exception.

32. (Original) The microcomputer according to claim 22, wherein the processor further comprises means for transmitting to the debug circuit address information of an executed instruction.

33. (Original) The microcomputer according to claim 22, wherein the processor includes means for transmitting to the debug circuit data information of an executed instruction.

34. (Original) The microcomputer according to claim 22, wherein the processor comprises means for transmitting to the debug circuit process identifier information of an executed instruction.

35. (Original) The microcomputer according to claim 22, wherein the debug circuit comprises means for transmitting processor control signals, including at least one of:

a signal to suspend operation of the processor;

a signal to resume fetching instructions;

a signal to reset the processor;

a signal to indicate that an exception has occurred in the debug unit.

36. (Original) The microcomputer according to claim 22, wherein at least one of the plurality of bit values represents a match state between a match value and a portion of an executed instruction.

37. (Original) The microcomputer according to claim 22, wherein at least one of the plurality of bit values represents a match state between a match value and a memory address accessed by the processor in response to an executed instruction.

38. (Original) The microcomputer according to claim 22, wherein the processor includes means for transmitting to the debug circuit a value indicating an increment of the program counter of the processor.

39. (Original) The microcomputer according to claim 22, wherein the processor is further configured transmit to the debug circuit a value indicating a change in process identifier value.

40. (Original) The microcomputer according to claim 22, wherein the debug circuit includes means for generating trace information including the program counter.

41. (Original) The microcomputer according to claim 22, wherein the microcomputer is implemented on a single integrated circuit.

42. (Currently amended) A method for transferring information between a processor and a debug circuit over a communication link, the method comprising:

transmitting to the debug circuit a plurality of bit values each representing a state of an operation in the processor including at least an ~~one of:~~ operand address; and

~~an operand address;~~

~~an instruction address, and;~~

transmitting a program counter value indicating the program counter of the processor.

43. (Original) The method according to claim 42, wherein at least one of the plurality of bit values represents a state of an operation in the processor including an operand value.

44. (Original) The method according to claim 43, wherein the program counter has a value corresponding to a value of the program counter at a writeback stage of a pipeline of the processor.

45. (Original) The method according to claim 44, the method further comprises a step of transmitting to the debug circuit a status indicating that a computer instruction is in the writeback stage is a valid computer instruction.

46. (Original) The method according to claim 44, the method further comprising a step of transmitting to the debug circuit a status indicating that the computer instruction in the writeback stage is a first instruction past a branch instruction.

47. (Original) The method according to claim 46, the method further comprising a step of transmitting to the debug circuit a status indicating a type of an executed branch instruction.

48. (Original) The method according to claim 47, the method further comprising a step of transmitting a trace packet indicating the type of the executed branch instruction.

49. (Original) The method according to claim 42, wherein the plurality of bit values representing a pre-execution state of the processor.

50. (Original) The method according to claim 42, the method further comprising a step of suppressing a transmission of the plurality of bit values upon detecting an exception.

51. (Original) The method according to claim 42, the method further comprising a step of transmitting to the debug circuit address information of an executed instruction.

52. (Original) The method according to claim 42, the method further comprising a step of transmitting to the debug circuit data information of an executed instruction.

53. (Original) The method according to claim 42, the method further comprising a step of transmitting to the debug circuit process identifier information of an executed instruction.

54. (Original) The method according to claim 42, the method further comprising a step of transmitting processor control signals, including at least one of:

a signal to suspend operation of the processor;

a signal to resume fetching instructions;

a signal to reset the processor;

a signal to indicate that an exception has occurred in the debug unit.

55. (Original) The method according to claim 42, wherein at least one of the plurality of bit values represents a match state between a match value and a portion of an executed instruction.

56. (Original) The method according to claim 42, wherein at least one of the plurality of bit values represents a match state between a match value and a memory address accessed by the processor in response to an executed instruction.

57. (Original) The method according to claim 42, the method further comprising a step of transmitting to the debug circuit a value indicating an increment of the program counter of the processor.

58. (Original) The method according to claim 42, the method further comprising a step of transmitting a value indicating a change in process identifier value to the debug circuit.

59. (Original) The method according to claim 42, the method further comprising a step of generating trace information including the program counter.

60. (Original) The method according to claim 42, wherein the microcomputer is implemented on a single integrated circuit.

61. (New) The microcomputer of claim 1, wherein the plurality of bit values further includes at least an instruction address.

62. (New) The microcomputer of claim 21, wherein the plurality of bit values further includes at least an instruction address.

63. (New) The microcomputer of claim 22, wherein the plurality of bit values further includes at least an instruction address.

64. (New) The method of claim 42, wherein the plurality of bit values further includes at least an instruction address.